

CLAIMS

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What is claimed is:

1. A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layer;

5 at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package, and the patterned circuit layer comprises at least a plurality of a first mounting pad and a plurality of a second mounting pad;
10 and

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package and a portion of the surface on the outer edge of the first mounting pad while exposing a portion of the surface of the first mounting pad and the whole surface of the second mounting pad.

Sub B²
15 2. The substrate structure of Flip Chip package of claim 1 wherein the material for the insulative layer is selected from the group consisting of "flame-retardant epoxy-glass fabric composite resin", Bismaleimide-Taiazine (BT), and epoxy.

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20 3. The substrate structure of Flip Chip package of claim 1 wherein each of the patterned circuit layer is formed by a copper foil layer defined by photolithographic and etching processes.

4. The substrate structure of Flip Chip package of claim 1 wherein the pitch of the first mounting pads is smaller than the pitch of the second mounting pad.

5. The substrate structure of Flip Chip package of claim 1 wherein a plurality of vias are disposed in the insulative layer for electrically connecting to the patterned circuit

layers.

6. The substrate structure of Flip Chip package of claim 1 wherein the first mounting pads are disposed on the periphery region of the substrate of the flip chip package while the second mounting pads are disposed in the central region of the substrate of the flip chip package.

7. A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layer;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package, and the patterned circuit layer comprises at least a plurality of a first mounting pad and a plurality of a second mounting pad;

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package and a portion of the surface on the outer edge of the first mounting pad while exposing a portion of the surface of the first mounting pad and the whole surface of the second mounting pad;

a chip having an active surface with a plurality of bumps disposed thereon wherein the chip has its active surface face to the surface of the substrate of the flip chip package, and the bumps are electrically connected to their corresponding first bonding pads and second bonding pads respectively; and

an underfill material filling between the active surface of the chip and the top surface of the substrate of the flip chip package.

8. The substrate structure of Flip Chip package of claim 7 wherein the material for the insulative layer is selected from the group consisting of "flame-retardant epoxy-

glass fabric composite resin", Bismaleimide-Taiazine (BT), and epoxy.

9. The substrate structure of Flip Chip package of claim 7 wherein each of the patterned circuit layer is formed by a copper foil layer defined by photolithographic and etching processes.

5 10. The substrate structure of Flip Chip package of claim 7 wherein the pitch of the first mounting pads is smaller than the pitch of the second mounting pad.

11. The substrate structure of Flip Chip package of claim 7 wherein a plurality of vias are disposed in the insulative layer for electrically connecting to the patterned circuit layers.

10 12. The substrate structure of Flip Chip package of claim 7 wherein the first mounting pads are disposed on the periphery region of the substrate of the flip chip package while the second mounting pads are disposed in the central region of the substrate of the flip chip package.

13. The substrate structure of Flip Chip package of claim 7 wherein the bumps attach only to the top surface of the first mounting pads.

14. The substrate structure of Flip Chip package of claim 7 wherein the bumps attach to both the top surface and side surfaces of the second mounting pads.

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